Claims 1, 6, and 15 are rejected under the second paragraph of 35 U.S.C. § 112

In the second and third enumerated paragraphs of the Office Action, the Examiner asserted that claims 1, 6 and 15 are indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In particular, the Examiner stated that the terms "short circuit or spare circuit," predetermined void," and "by way of predetermined void" are not understood. This rejection is respectfully traversed.

Initially, Applicant notes that the terms "short circuit or spare circuit" have been deleted from the claims. As such, the Examiner's rejection, as pertaining to these terms, has been rendered moot

With regard to the terms "predetermined void" and "by way of predetermined void," Applicant notes that the Examiner has failed to establish a prima facie case of indefiniteness under 35 U.S.C. § 112. The Examiner has merely asserted that these terms are not understood without establishing (a) an interpretation of the claim in light of the specification; (b) an interpretation of the claim as interpreted by one of ordinary skill in the art; and (c) that the limitation(s) in the claim does not reasonably define the invention. **See** M.P.E.P. § 2173.02. Notwithstanding that the Examiner has not explained why these terms are not understood, Applicant refers the Examiner to page 9, lines 7-18 of Applicant's specification, in which the "void" is discussed. With regard to the term "by way of," Applicant notes that this term connotes an intermediate feature between other features. Accordingly, claim 1 has been amended so that the limitation "a second interconnection formed on said plug by way of a predetermined void" is now recited as "a predetermined void between said plug and said second interconnection."

Applicant's position is that that one having ordinary skill in the art would have no difficulty understanding the scope of claims 1, 6, and 15, particularly when reasonably interpreted in light of the written description of the specification. **In re Okuzawa**, 537 F.2d 545, 190 USPQ 464 (CCPA 1976); **In re Royka**, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Thus, the imposed rejection of claims 1, 6, and 15 under the second paragraph of 35 U.S.C. § 112 have been overcome and, hence, Applicant respectfully solicits withdrawal thereof.

Claims 1-6 are rejected under 35 U.S.C. § 102(b) for lack of novelty as evidenced by Sur, Jr. et al., U.S. Patent No. 5,764,563 (hereinafter Sur 1)

In the sixth enumerated paragraph of the Office Action, the Examiner asserted that Sur 1 discloses a semiconductor device corresponding to that claimed. This rejection is respectfully traversed.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that one having ordinary skill in the art would have recognized that the identically claimed invention is within the public domain. **ATD Corporation v. Lydall, Inc.**, 159 F.3d 534, 48 USPQ2d 1321 (Fed. Cir. 1998); **Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.**, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994). Accordingly, in deciding the issue of anticipation, the Examiner is burdened to (a) identify the elements of the claims, (b) determine the meaning of the elements in light of the specification and prosecution history, and (c) identify corresponding elements disclosed in the allegedly anticipating reference. **Lindermann Maschinenfabrik GMBH v.**

American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). This burden has not been discharged.

Independent claims 1 and 6 both recite a predetermined void. In the statement of the rejection, the Examiner asserted that Sur 1 teaches:

> a second interconnection 240 ... formed on said plug by way of a determined [sic] void ... [and a] second dielectric film 346 having a predetermined void located at a position above said plug (as in claim 6) and covering said second interconnection.

The Examiner is referred to 37 C.F.R. § 1.104(c), which is reproduced below:

> In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified. (emphasis added)

Although the Examiner has asserted that a predetermined void is disclosed by Sur 1, the Examiner has failed to designate which feature in Sur 1 is being relied upon by the Examiner for this disclosure. Notwithstanding the Examiner's failure to identify a predetermined void in Sur 1, Applicant respectfully submits that Sur 1 does not disclose a predetermined void. Therefore, Sur 1 fails to identically describe the claimed invention.

The above argued differences between the semiconductor device defined in independent claim 1 and the device of Sur 1 undermine the factual determination that Sur 1 identically describes the claimed invention within the meaning of 35 U.S.C. § 102. **Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc.**, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); **Kloster Speedsteel AB v. Crucible Inc.**, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). Applicant, therefore, respectfully submits that the imposed rejection of claims 1-6 under 35

U.S.C. § 102 for lack of novelty as evidenced by Sur 1 is not factually viable and, hence, solicit withdrawal thereof.

Claims 1-2 and 4-6 are rejected under 35 U.S.C. § 102(b) for lack of novelty as evidenced by Gordon et al., U.S. Patent No. 5,786,268 (hereinafter Gordon)

In the seventh enumerated paragraph of the Office Action, the Examiner asserted that Gordon discloses a semiconductor device corresponding to that claimed. This rejection is respectfully traversed.

As with Sur 1, the Examiner has also failed to indicate which feature in Gordon is being relied upon by the Examiner for the disclosure of a predetermined void, as recited in independent claims 1 and 6. Notwithstanding the Examiner's failure to identify a predetermined void in Gordon, Gordon does not disclose a predetermined void. Applicant, therefore, respectfully submits that the imposed rejection of claims 1-2 and 4-6 under 35 U.S.C. § 102 for lack of novelty as evidenced by Gordon is not factually viable and, hence, solicit withdrawal thereof.

Claims 1 and 6 are rejected under 35 U.S.C. § 102(b) for lack of novelty as evidenced by Sur, Jr. et al., U.S. Patent No. 6,143,642 (hereinafter Sur 2)

In the eighth enumerated paragraph of the Office Action, the Examiner asserted that Sur 2 discloses a semiconductor device corresponding to that claimed. This rejection is respectfully traversed.

In the statement of the rejection, the Examiner identified feature 320 in Sur 2 as being comparable to the claimed predetermined void. Initially, Applicant notes that the Examiner has failed to determine the meaning of the term "predetermined void" in light of the specification and prosecution history. **Lindermann Maschinenfabrik GMBH v. American Hoist & Derrick Co., supra**. This is evidenced by the Examiner admitting in the statement of the rejection to not understanding the term "predetermined void," even though as previously argued, the specification clearly defines the term such that one having ordinary skill in the art would have no difficulty understanding this term.

Feature 320 in Sur 2 is described as a gap 320 (column 5, lines 52-56; Fig. 3C). In contrast to the predetermined void recited in claims 1 and 6, the gap 320 of Sur 2 is merely a portion of a plug 312 that is not covered by a metallization layer 314. As illustrated in Fig. 3F, an inter-metal oxide 317 will completely cover the substrate 300 so that no void is present. As such, Sur 2 does not disclose a predetermined void, as recited in claims 1 and 6. Applicant, therefore, respectfully submits that the imposed rejection of claims and 6 under 35 U.S.C. § 102 for lack of novelty as evidenced by Sur 2 is not factually viable and, hence, solicit withdrawal thereof.

Claim 15 is rejected under 35 U.S.C. § 102(e) for lack of novelty as evidenced by Anma et al., U.S. Patent No. 6,319,812 (hereinafter Anma)

In the ninth enumerated paragraph of the Office Action, the Examiner asserted that Anma discloses a semiconductor device corresponding to that claimed. This rejection is respectfully traversed.

As with Sur 1 and Gordon before it, the Examiner has also failed to indicate which feature in Anma is being relied upon by the Examiner for the disclosure of a predetermined void, which is also recited in independent claim 15. Notwithstanding the Examiner's failure to identify a predetermined void in Anma, Anma does not disclose a predetermined void. Applicant, therefore, respectfully submits that the imposed rejection of claim 15 under 35 U.S.C. § 102 for lack of novelty as evidenced by Anma is not factually viable and, hence, solicit withdrawal thereof.

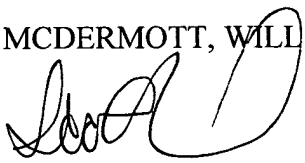
Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing remarks, Applicant hereby respectfully requests reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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Version with markings to show changes made

IN THE CLAIMS:

Please amend claims 1, 6 and 15 as follows:

1. (Amended) A semiconductor device [having a short circuit or a spare circuit for preventing application of a high voltage to a load circuit] comprising:

a substrate;

a first interconnection formed on said substrate [and connected to the short circuit or the spare circuit];

a first dielectric film [for] covering said first interconnection;

an opening section [for] extending from a surface of the first dielectric film to said first interconnection, said opening section being formed in said first dielectric film;

a plug formed in said opening section and electrically connected to said first interconnection;

a second interconnection formed [on] over said plug; [by way of]

a predetermined void between said plug and said second interconnection [and connected to the load circuit]; and

a second dielectric film [for] covering said second interconnection.

6. (Amended) A semiconductor device [having a short circuit or a spare circuit for preventing application of a high voltage to a load circuit] comprising:

a substrate;

a first interconnection formed on said substrate [and connected to the short circuit or the spare circuit];

a first dielectric film [for] covering said first interconnection;

an opening section [for] extending from a surface of said first dielectric film to said first interconnection, said opening section being formed in said first dielectric film;

a plug formed in said opening section and electrically connected to said first interconnection;

a second interconnection formed on said first dielectric film in the vicinity of said plug [and connected to the load circuit]; [and]

a second dielectric film [having] covering said second interconnection; and

a predetermined void in said second dielectric film and located at a position adjacent to said second interconnection and at a position above said plug [, said second dielectric film covering said second interconnection].

15. (Amended) A semiconductor device [having a short circuit or a spare circuit for preventing application of a high voltage to a load circuit] comprising:

a substrate;

a first dielectric film formed on said substrate and having an opening section;

a pad formed in the opening section and having conductivity;

a first interconnection formed on said first dielectric film such that a portion of a bottom of said first interconnection comes into contact with an upper surface of said pad;

a second interconnection formed on said first dielectric film such that a bottom surface of said second interconnection does not come into contact with the upper surface of said pad, [said second interconnection being connected to the load circuit,] said pad being disposed between said first and second interconnections; and

a second dielectric film [having] covering said first and second interconnections; and

a predetermined void in said second dielectric film and located at a position on said pad [, said second dielectric film covering said first and second interconnections].